WHAT IS CLAIMED IS:

1. A switching fabric comprising:

a plurality of cross points that process multiple stripes of serial data; and

wherein each cross point includes a plurality of port slices.

2. The switching fabric of claim 1, wherein said plurality of cross points comprise five cross points.

3. The switching fabric of claim 1, wherein each cross point comprises:

a plurality of ports; and

a plurality of port slices coupled respectively to said ports.

4. The switching fabric of claim 1, wherein each port slice comprises:

a plurality of FIFOs coupled to other ones of said port slices; and

a FIFO read arbitrator coupled to each FIFO, wherein said FIFO read arbitrator arbitrates read requests sent by said FIFOs.

5. The switching fabric of claim 4, wherein each port slice further comprises:

a multiplexer coupled to said FIFOs and to said FIFO read arbitrator; and

a dispatcher coupled to an output of said multiplexer.

6. The switching fabric of claim 1, wherein each port slice comprises:

an accumulator that writes received data to an appropriate FIFO in a different port slice.

7. The switching fabric of claim 1, wherein each cross point comprises eight ports and eight port slices.

8. A cross point that processes a stripe of serial data, comprising:

a plurality of ports; and

a plurality of port slices coupled respectively to said ports.

9. The cross point of claim 8, wherein each port slice comprises:

a plurality of FIFOs coupled to other ones of said port slices; and

a FIFO read arbitrator coupled to each FIFO, wherein said FIFO read arbitrator arbitrates read requests sent by said FIFOs.

10. The cross point of claim 9, wherein each port slice further comprises:

a multiplexer coupled to said FIFOs and to said FIFO read arbitrator; and

a dispatcher coupled to an output of said multiplexer.

11. The cross point of claim 9, wherein each port slice comprises:

an accumulator that writes received data to an appropriate FIFO in a different port slice.

12. The cross point of claim 8, wherein each cross point comprises eight ports and eight port slices.

13. A method for processing a stripe of data at a cross point, comprising, at one port slice:

storing data received from other port slices in a plurality of FIFOs; and

arbitrating the reading of the stored data.

14. The method of claim 13, further comprising:

writing data received from a port at the one port slice to an appropriate FIFO in a different port slice.

15. A method for processing data in port slice based on wide cell encoding and an external flow control command, comprising:

managing 64-bit entries in a receive synch FIFO;

receiving two chunks of 32-bit data from the receive synch FIFO;

detecting a K0 in a first byte of the received two chunks of 32-bit data; and

extracting a destination slot from a state field in a cell header when K0 is detected.

16. The method of claim 15, further comprising:

determining whether the cell header is low-aligned or high-aligned;

writing 64-bit data to a data FIFO corresponding to the destination slot when the cell header is either low-aligned or high-aligned;

writing two 64-bit data to two data FIFOs corresponding to the two destination slots when the cell header is low-aligned and high-aligned; and

filling the second chunk of 32-bit data with idle characters when a cell does not terminate at the 64-bit boundary and a subsequent cell is destined for a different slot.

17. The method of claim 16, further comprising:

performing an early terminate to a cell that inserts K0 and ABORT state information in the data when an error condition is detected.

18. The method of claim 16, further comprising:

stopping requests to a FIFO read arbitrator after a current cell is completely read from a FIFO RAM when a flow control condition is detected.

19. The method of claim 16, further comprising:

delivering 64-bit data to a SERDES synch FIFO module and transmitter when non-idle data is received from a FIFO read arbitrator;

injecting a first alignment sequence to be transmitted to the SERDES synch FIFO module and transmitter when the FIFO read arbitrator indicates that a plurality of FIFO RAMs are empty

injecting a second alignment sequence to be transmitted to the SERDES transmitter when a programmable timer expires and a previous cell has been completely transmitted; and

indicating to the FIFO read arbitrator to temporarily stop serving any requestor until a current pre-scheduled alignment sequence has been completely transmitted.